IN THE CLAIMS:

Claim 1 (currently amended) A multilayered wiring structure for high frequency semiconductor devices, comprising:

a semiconductor substrate;

a ground plate formed above said semiconductor substrate, having a potential fixed at the ground potential;

a plurality of wiring layers, each of which is alternately stacked with an insulating interlayer formed above said semiconductor substrate, the wiring layers combining with said ground plate to form transmission lines; and

at least one separation electrode being selectively provided on the additional insulating interlayers, said at least one separation electrode having a potential fixed at the ground potential;

wherein said at least one separation electrode is formed near the crossing portion where the wiring layers mutually cross, with insulating interlayers provided therebetween.

Claim 2 (currently amended) A multilayered wiring structure for high frequency semiconductor devices, according to Claim 1, wherein the ~~size~~ length and width dimensions of said at least one separation electrode ~~is~~ are sufficiently smaller than the length of each of the wiring layers used in forming the transmission lines above said semiconductor substrate so as to not significantly interfere with transmission line characteristics of the wiring layers.

Claim 3 (currently amended) A multilayered wiring structure for high frequency semiconductor devices; according to Claim 1, further including additional crossing portions where the wiring layers mutually cross, wherein each of the crossing portions has ~~the~~ an individual separation electrode.

Claim 4 (currently amended) A multilayered wiring structure for high frequency semiconductor devices; according to Claim 3, wherein the separation electrodes are electrically interconnected.

Claim 5 (currently amended) A multilayered wiring structure for high frequency semiconductor devices; according to Claim 3, wherein the separation electrodes have a potential which is fixed at the ground potential by a common electrode.

Claim 6 (currently amended) A multilayered wiring structure for high frequency semiconductor devices; according to Claim 4, wherein the separation electrodes are provided on one of the insulating interlayers, and are electrically interconnected by wiring extended on said insulating interlayer.

Claim 7 (currently amended) A multilayered wiring structure for high frequency semiconductor devices; according to Claim 4, wherein the separation electrodes are provided on

different insulating interlayers, and are electrically interconnected by at least one ~~throughhole~~ through-hole.

Claim 8 (currently amended) A multilayered wiring structure for high frequency semiconductor devices, according to Claim 1, wherein a single separation electrode is ~~in common~~ provided for all of the crossing portions.

A16 end

Claim 9 (currently amended) A multilayered wiring structure for high frequency semiconductor devices, according to Claim 3, wherein the crossing portions are positioned at different levels, and the separation electrodes are provided on those of the insulating interlayers which are provided ~~in common in~~ for all of the crossing portions.

Claim 10 (currently amended) A multilayered wiring structure for high frequency semiconductor devices, according to Claim 8, wherein the crossing portions are positioned at different levels, and said single separation electrode is provided on one of the insulating interlayers which is provided ~~in common in~~ for all of the crossing portions.